NOVEL DESIGN OF A DIGITAL PLL FOR POWER REDUCTION

SHORT SYNOPSIS

Submitted in partial fulfillment of the requirement of the degree of

DOCTOR OF PHILOSOPHY

to

Manav Rachna International Institute of Research and Studies

(Deemed to be University)

by

Shruti Hathwalia
17/Ph.D/036 (FET)

Under the supervision of

Dr. Naresh Grover

Dean – Academics, MRIIRS

FACULTY OF ENGINEERING & TECHNOLOGY

MANAV RACHNA INTERNATIONAL INSTITUTE OF RESEARCH & STUDIES

SECTOR-43, SURAJKUND –DELHI ROAD, FARIDABAD – 121001

FACULTY OF ENGINEERING & TECHNOLOGY

Certificate

I hereby declare that the short synopsis "**NOVEL DESIGN OF A DIGITAL PLL FOR POWER REDUCTION** "being submitted in partial fulfillment of the requirement for the degree of Doctor of Philosophy in Electronics & Communication under Faculty of Engineering & Technology of Manav Rachna International Institute of Research & Studies, Faridabad during the academic year 2017-2020.

It is a bona fide record of original work carried out under the supervision of Dr.Naresh Grover and has not been submitted in full or part to any other university or institute for degree or diploma. Further, it is certified that short synopsis is plagiarism free and proof has been submitted.

Shruti Hathwalia
17/Ph.D/036

11/6/2019
Dr.Naresh Grover
Dean - Academics
MRIIRS

(Chairman, DRC)

Chairperson, CDP

ABSTRACT

Very large scale integration (VLSI) circuits operating at ultra low power are currently acquiring more attention from the research group and the industries too. Recently, the performance of many applications depends on the size and energy consumption of sensor nodes. The energy efficient sensor nodes with reduced size are much preferred among applications such as wireless sensor networks, pollution and plant monitoring, biomedical, smart grids. In present day digital systems, clocks are used for sequencing their operations and they also help in synchronization between different functional units. The biggest challenge faced by the VLSI designers in present day life is designing a product of new generation which operates on minimum possible power. The new generation of designers should follow the design culture. Power consideration is the eventual design criteria in different real life applications like pacemakers etc. The main objective of all these applications is minimum power and maximum battery lifetime. Phase Locked Loop is a framework that produces an output which is in phase with the input signal. In Phase Locked Loop (PLL), the focus is at the input signal's phase with its output oscillator signal's phase and thus modifies the recurrence frequency of the Voltage Controlled Oscillator (VCO) for phase co-ordination. The output signal from the Phase Frequency Detector is utilized to control the oscillator in a feedback circle. Generally, in high performance based advanced frameworks, PLLs are utilized so as to create on-chip clocks. Likewise, as an operational gadget, the PLL has wide scope of utilization in media transmission, PCs and electronic applications.

In the proposed work, designing and analysis of PLL with numerous outputs is to be implemented by changing the closed loop frequency control framework PLL blocks. As such, high effective, low power, ideal area chip can be used for PLL with four various yields as PLL 8x, PLL 4x, PLL 2x and PLL 1x with different frequencies separately. Likewise, it is planned to utilize multi-threshold or sleep transistors to minimize the leakage current in the circuit. Further, the execution or performance verification of various parameters of PLL will be done to acquire negligible power.

Key words: Phase Locked Loop (PLL), Optimization Techniques, Power Dissipation, Flip-Flops, Ultra low power, Voltage controlled oscillator (VCO), multiple outputs.

CONTENTS

S.No.	Description	Page No.
	Abstract	iii
1.	Introduction	1-2
2.	Literature Review	3-5
2.1	Gaps in Literature	5
3.	Description of Broad Area	6-7
4.	Objectives of the study	8
4.1	Problem Statement	8
4.2	Objectives of Research	8
5.	Research Methodology	8-10
6.	Expected Outcome	11
7.	References	12-13

1. INTRODUCTION

The greatest challenge looked by the VLSI creators today is structuring a new product which devours least power. For preserving the power, it is required to achieve it with high performance or minimal area. The new generation of designers should follow the design culture. The power consideration is the eventual design criteria in different real-life applications namely wristwatches etc. The main objective of all these applications is minimal power and utmost possible battery lifetime. Low power design is required to reduce the power of the high-performance systems (Bellaouar, Elmasry, 1995). PLL is a feedback system in which the produced output signals are phase-locked with the input signals given externally. Tracking of input signals in frequency and phase is done by PLL. Some of the applications of PLL include tracking filter, frequency shifting decoding for demodulation of carrier frequencies etc. The digital PLL is one of the types of PLL which uses both combinations of digital as well as analog techniques to achieve powerful operation of the devices (Akila, 2004). Scaling of CMOS devices, has led the digital Phase locked loop (PLL) to increase its market share in wi-fi trans-receivers.

In past few years, two types of digital PLL that have been developed are **fractional N divider digital PLL** and **counter-based digital PLL** (Maffezzoni, P., Marucci, G., Levantino, S., & Samori, C. 2013). Counter based PLL is used in WPAN applications. Traditional counter based PLL performs the frequency digitizing through the high-speed counter along with the TDC (time to digital converter). In practical digital circuits, power dissipation is caused due to signal transition, short circuit current and leakage currents. For now, as the technology grows, short circuit and leakage currents have become the main concern (Kao, Chandrakasan 2000; Sirisantana, 2000).

Working Methodology of PLL

Phase Locked loop is one of the fundamental squares in present day electronic frameworks. It is commonly utilized in sight and sound, correspondence and in numerous different applications.

A PLL is a feedback system that includes following blocks:

1. PFD $\Longrightarrow$ Phase Frequency detector
2. LPF $\Longrightarrow$ Low pass filter
3. VCO $\Longrightarrow$ Voltage controlled oscillator

The motivation is to drive the VCO to duplicate and track the recurrence (frequency) and stage (phase) at the information (input) when in lock state. The PLL is a control framework enabling one oscillator to follow another.

Further, block diagram of a PLL is shown in the diagram below.

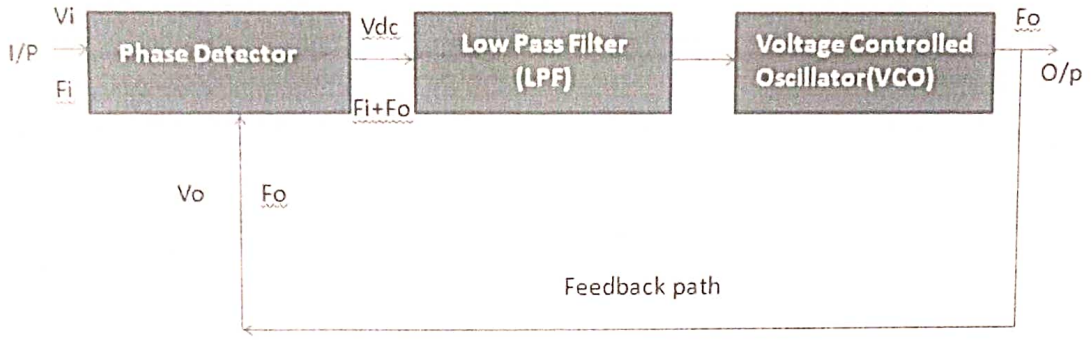

Figure 1 Phase Locked Loop Block Diagram

In Figure 1 given above, the info signal (Vi) with information recurrence (Fi) is yielded by a phase detector (PFD) in a PLL. PFD is a comparator, looking at the information recurrence (Fi) through the input recurrence (Fo). The yield of PFD (Fi+Fo) is a DC voltage. At that point, the yield of PFD is passed to Low Pass Filter which removes the high recurrence noise and creates a steady DC level (Fi-Fo). Further, the yield of low pass filter is passed to Voltage controlled oscillator (VCO). The information signal (Fi) is relative to the yield of VCO (Fo). The information and yield frequencies are analyzed and balanced through the feedback loop until the yield recurrence (Fo) = input recurrence (Fi).

In this way, it is obvious from the above working methodology that PLL works like free running, catch and stage lock. Therefore, when there is no input voltage connected, PLL is said to work in free running stage. While, whenever input recurrence (Fi) is connected, VCO changes and creates a yield recurrence (Fo) for examination, PLL is said to be in catch organize. This computerized PLL is utilized in planning of the VLSI circuits to decrease the power and increment the presentation of the circuit.

2. LITERATURE REVIEW

Very large scale integration (VLSI) circuits operating at ultra-low power are currently acquiring more attention from the research group and the industries too. Recently, the performance of many applications depends on the size and energy consumption of sensor nodes. The energy efficient sensor nodes with reduced size are much preferred among applications such as wireless sensor networks, pollution and plant monitoring, biomedical, smart grids etc. Digital VLSI circuits are also used in improving the digitally-aided circuit blocks in analog and RF domains (Alioto, 2012).

Chung & Lee (2003) proposed a novel all-digital phase locked loop (ADPLL) in which there was fine adjusting of the delay cell. Proposed frequency tracking algorithm is reviewed and verified using TSMC CMOS process standard cells with 3.33V supplied power. The ADPLL architecture is proposed with the filter and the controller which reduced the power consumption. The proposed cell-based Digital controlled oscillator was designed which has two stages such as coarse tuning stage and fine-tuning stage. The results show that the response of the DPLL with reference clock is 5 MHz. The ADPLL implementation with the standard cell is shown, and it reduced the design-time and circuit complexity.

Jasmin (2014) has reviewed and considered power consumption in different system levels. Techniques such as combinational logic optimization were used. Different techniques were followed for the optimization such as path balancing, retiming, and factorization, technology mapping, sequential circuit encoding, pre-computation and gated clocks. The device level and layout level for power optimization were left unexplained in the paper. The main focus was on power optimization at different levels of abstractions.

The power enhancement at the circuit dimension of a counter which is fast and a retiming circuit which is aimed for ultra-low power DPLL is clarified by the creators Pereira, M. & Vaz, J. C. (2018). The asynchronous type of rapid counter is given exact inspecting stage generator. To get the low power arrangement non-concurrent counter topologies have been utilized (Wu, Shahmohammadi, Chen, Lu, & Staszewski 2017). In asynchronous counter the main flip flop is timed by the RF oscillator which helps in enormous power reserving.

The clock system consisting of clock linking networks and timing components such as flip-flops and latches are estimated to be the more power consuming components in VLSI system, around 30 to 60 percent of total energy in a system. Also to gain high-performance circuit, a number of clock networks were used resulting in high power consumption. Hence, limiting the power consumption

in flip-flops becomes a crucial factor. The design of the CMOS charge pumps is used in the CMOS circuits with phase locked loop applications (Rhee, 1999).

Ramkanth & He (2014) proposed a standard recurrence synthesizer, where high yield current of the charge pump provided better upgrade achievement over the leakage current and thus had high signal to noise ratio (SNR). The present usage of the charge pump is less than a few 100 microamperes in the tri-state operation. Different types of charge pumps are reviewed and have various applications such as digital clock generators, frequency synthesizers etc. and the design issues along with selecting the environment of PLL and other requirements like maximum leakage current ground noise rejection. PLL in this work is used for the design of the charge pump architecture. The structuring of analog phase locked loop is based on feedback loop which is controlled carefully. The information is locked by the digital control loop. The design of the PLL for circuit applications with low power is quite important where the different types of oscillators and passive components of the integrated circuits are required to work in the system.

Yang (2010) presented a 10 GHz system with dynamic digital loop filter using all digital frequency synthesizers (ADPLL). Digital loop filter was recomposed mechanically by a locking process monitor (LPM) during the frequency gain and phase finding process. During the locking process, the loop bandwidth is automatically configured to attain quick lock and lower noise together. A phase accumulator which is skew-compensated was introduced to maintain the benefits of low power dissipation and to achieve high-speed operation simultaneously solving the accumulated timing skew issue.

Sangeeta (2013) proposed an efficient technique of multi-threshold voltage CMOS for reducing leakage power. The digital circuit NAND gate was implemented with leakage reduction techniques. It was concluded that the leakage power of all the designs decrease when reduction techniques are applied. The results also showed that percentage reduction of leakage power was more with MTCMOS techniques in comparison to the stacking technique.

Bipin Gupta & Sanjay Rajak (2014) analyzed the leakage feedback power decrease system in CMOS circuit and confirmed that strategy on D flip-flop, PFD and essential charge pump circuit. Likewise, the already existing leakage power control strategies in CMOS circuit were analyzed. The outcomes demonstrated that on applying the proposed technique on D flip-flop and PFD, there was a significant decrease in standby power. Power and delay were likewise observed to be decreased to an incredible dimension.

Ujwala A. Belorkar (2011) introduced an area efficient design for 3.3GHz PLL with four various outputs. VLSI Technology including process configuration, patterns, chip creation, circuit plan and reasonable involvement in format configuration were utilized. The proposed PLL was structured utilizing 45nm CMOS innovation with microwind 3.1. High effective, low power ideal region chip was intended for PLL with 4 yields of 3.3GHz, 1.65GHz, 0.825GHz and 0.412GHz.

2.1 Gaps in Literature

At circuit level, a counter which is rapid and a retiming circuit that is gone for low power digital Phase Locked Loop (DPLL) has yet not been designed. There are many techniques for leakage power reduction for VLSI applications. On the basis of literature, it is found that for larger leakage power savings, the Multi-threshold CMOS (MTCMOS) method is most preferred. Power dissipation is extremely pivotal with the development rate of batteries. Also, use of multiple outputs PLL provides clock generation as compared to single output PLL. In present day communication applications with low power, high steadiness and low jitter, multiple output unit of PLL is preferred.

3. DESCRIPTION OF BROAD AREA

The growth of competitive market sectors like wireless applications depends on the power dissipation as the most critical criterion since the growth rate of the batteries is not convincing. Thus, the power optimization is considered as an essential factor. By concentrated planning, skew will surpass only one information clock period which causes failure and meta-steadiness issues inside sampling process. Though fully synthesis standard-cell libraries have prompted extravagant power usage for ultra low power genuine applications. The real test is selecting the right True Single Phase Clock (TSPC) structure for the correct place.

In VLSI circuits operating at ultra-low power, the performance majorly depends on:

- Size of the sensor node
- Energy consumption

In this way these circuits have wide applications in remote sensor network, pollution, biomedical and so forth. For remote applications, power dissipation is extremely pivotal since development rate of batteries isn't persuading. Thus power optimization is a must.

A. Phase Frequency Detector (PFD)

A standout amongst the most vital segments of PLL and DLL which is frequently considered as the bottleneck is the Phase Frequency Detector. Restricted speed of this square is the principle constraining variable in the data rate of PLL. PFD is a comparator of input and feedback frequency. In high frequency, PFD can't follow the phase differences among reference and feedback clocks. Thus, **Frequency divider circuit** is embedded before the PFD block in the feedback way of PLL. It implies that the input clock frequency of the PFD is decreased. In any case, by including the divider circuit, the general jitter of the PLL will be very high.

Along these lines, advantages of structuring a high recurrence PFD are:

1. The divider circuit will be removed.
2. Noise conduct of the PLL will be improved.

Generally, there are 2 kinds of Phase Detectors utilized in the circuits: **XOR Phase Detector** (least difficult structure) and **Phase frequency detector** (most normal structure which unravels the weaknesses of XOR).

B. Voltage Controlled Oscillator(VCO)

The VCO is the most essential practical unit in the PLL. Its output frequency decides the viability of PLL. Notwithstanding working at highest frequency, this unit consumes a large portion of the power in the framework. VCO is of specific importance for reducing the power consumption in PLL. Generally, PLL with numerous outputs means VCO having multiple outputs.

There are different issues found in the effectively existing VCO:-

Issue 1

One issue with the conventional phase noise estimations of VCO is that the output frequency of the gadget when they are not locked by PLL drifts generously over the estimation time. The VCOs are exceptionally sensitive gadgets and they experience drift because of little thermal changes and even vibrations. This carrier drift creates a noteworthy error that can only be rectified through broad averaging.

Issue 2

Another issue is the noise measurement range. Analyzers are utilized to measure the phase noise in PLL circuits. Beside the drift issue referenced above, Spectrum analyzers don't have a low enough noise floor to assess a significant number of the devices required in the present communication frameworks.

Performance verification check of the measurement framework, after each connection change is important for repeatable estimations. At the point when the loop filter attributes or oscillation recurrence is changed, measurement estimation and setup should also likewise be changed. This tedious work may result in long item development time. Since the PFD in a PLL is set to an ideal frequency, by carefully controlling the PLL IC chip, a PLL control program is vital. In this manner, it is difficult to begin the synthesizer assessment until either a control circuit or the program is finished. Since it is hard to synchronize estimations with the PLL frequency change, PLL lock time estimation precision is hard to accomplish.

4. OBJECTIVES OF THE STUDY

4.1 Problem Statement

The main objective of this work is to design, implement and analyze a robust Phase Locked Loop (PLL) with four various yields as PLL 8x, PLL 4x, PLL 2x and PLL 1x with different frequencies separately. Different blocks of PLL are to be designed. Likewise, to utilize multi-threshold (MTCMOS) or sleep transistors method to minimize the leakage current in the circuit is also planned. Further, the execution or performance verification of various parameters of PLL will be done to acquire negligible power. Finally, the proposed circuit will be compared with the already existing work in same field.

4.2 Objectives of the research shall be:

1. To design a high frequency Phase frequency detector (PFD) & charge pump.
2. To design Low power filter & high performance LC-VCO.
3. To design the multiple output unit of PLL (PLL with 4 Outputs).
4. To measure the performance verification of the circuit for different parameters.
5. To compare the proposed circuit with already existing work.

5. RESEARCH METHODOLOGY

Power advancement of a counter at circuit level which is rapid and a retiming circuit that is gone for low power DPLL is proposed in the low-control differential voltage-controlled oscillator (LP-VCO) PLL circuit. A high-speed counter is added into an Asynchronous counter-based digital PLL. Asynchronous counter topology is preferred as its power consumption is very less. The primary flip-flop is alone clocked by RF oscillator in asynchronous counters attributable to noteworthy power savings. Additionally, the sample phase generator (SPG) sampling method could be used to analyze voltage temperature (PVT). At the common-source node, the introduced LP-VCO is very immune to the phase noise created by other components.

In the flowchart given below, the brief methodology of work to be done is shown:

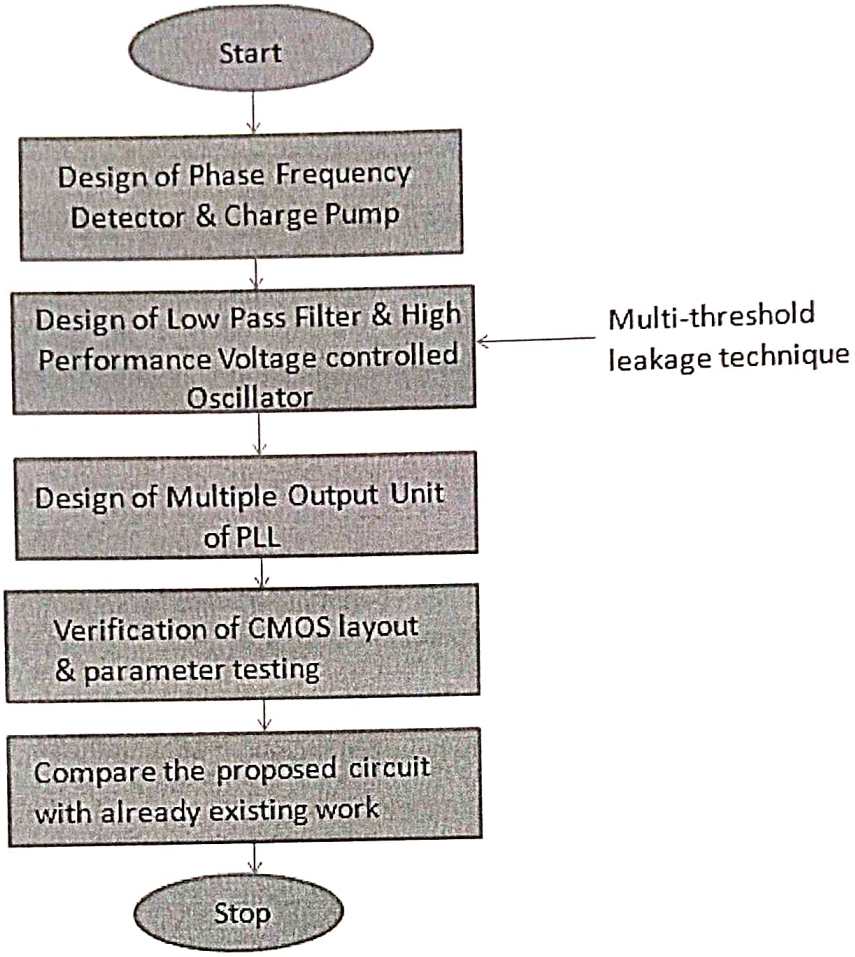
Start
Design of Phase Frequency Detector & Charge Pump
Design of Low Pass Filter & High Performance Voltage controlled Oscillator
Multi-threshold leakage technique
Design of Multiple Output Unit of PLL
Verification of CMOS layout & parameter testing
Compare the proposed circuit with already existing work
Stop

Figure 2 Methodology flowchart

A. Low Power-Voltage Controlled Oscillator (LP-VCO)

The LP-VCO oscillator builds a parallel resonance tank using an inductor and a capacitor. Active elements such as resistor are used to compensate the losses of the inductor and the capacitor. Since the capacitance depends on the tuning input voltage, the circuit introduces a VCO with the angular centre frequency. LC-VCO PLLs are mostly used in high-performance RF systems due to their ultra-low phase noise and energy dissipation than ring VCOs. LC-VCO PLLs can be used for a high-frequency operation. (Tiebout, 2001; Wu, 2009; Yun, 2005).

B. Multi-threshold Leakage Technique or Sleeping Transistor

The multi-threshold voltage CMOS (MTCMOS) method or sleep transistor is utilized in order to minimize the leakage current in a circuit. This is a sort of power gating method which utilizes high threshold transistor as a sleep transistor and low threshold voltage transistors are utilized in logic implementation. MTCMOS is a viable procedure which improves the performance in dynamic mode and saves the leakage power in standby mode. Essential principle of the MTCMOS strategy is to bring down the threshold to structure the logic gates where the switching speed is imperative while the high threshold transistors, additionally called the sleep transistors are utilized to adequately detach the logic gates in standby mode. With the introduction of sleep transistor, the obstruction path amid standby mode of activity results in decrease of leakage current.

MTCMOS is a variety of CMOS chip innovation which has transistors with various thresholds, so as to optimize power and delay. Low threshold gadgets switch quicker and are in this way helpful on basic delay paths to limit clock periods. On the other hand, high threshold devices decrease static leakage by 10 times in contrast with low threshold devices.

C. Multiple Output unit

Multiple outputs PLL provides clock generation. It is expected to structure PLL with various outputs for present day communication applications with low power, high steadiness and low jitter. For multiple outputs PLL, 1x is the fundamental output; the 90° phase moved output is created utilizing delay circuits which thusly offers speed execution at low power.

Figure 2. appeared beneath depicts the block diagram of 4 yields PLL with performance VCO. The yields are 1x, 2x, 4x and 8x which can be used in multiphase timing circuits.

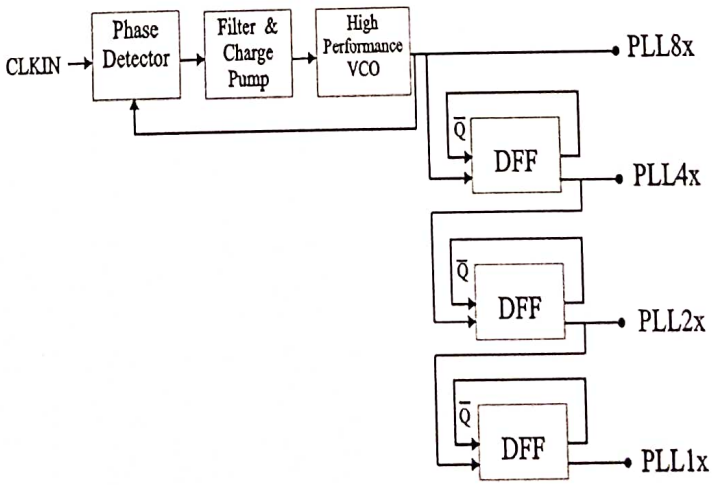

Figure 3 Block schematic of PLL with four outputs

6. EXPECTED OUTCOME

In the proposed work, it is intended to utilize multi-threshold or sleep transistors to decrease the leakage current. Design and analysis of low power PLL with different outputs is fundamentally implemented by adjusting closed loop frequency of PLL blocks. Along these lines high effective, low power, ideal area chip can be intended for PLL with different outputs as PLL 8x, PLL 4x, PLL 2x and PLL 1x at the same time. Frequencies of the outputs can be settled on later stage.

1) A new PLL circuit with minimum power consumption, high speed & maximum battery life is to be designed for use in real life wireless applications.
2) The proposed research solves the issues in existing technique and improves the power dissipation problem by employing LC-VCO in PLL circuit to reduce the phase noise in VCO circuits.
3) The verification of CMOS layout & parameter testing has to be done.
4) Once we achieve the goal for the given parameters including detailed verification stop the design analysis and after that our design can be used for IC making.

7. REFERENCES

Alioto, M., 2012. Ultra-low power VLSI circuit design demystified and explained: A tutorial. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *59*(1), pp.3-29.

Babaie, M., Kuo, F.W., Chen, H.N.R., Cho, L.C., Jou, C.P., Hsueh, F.L., Shahmohammadi, M. and Staszewski, R.B., 2016. A fully integrated Bluetooth low-energy transmitter in 28 nm CMOS with 36% system efficiency at 3 dBm. *IEEE Journal of Solid-State Circuits*, *51*(7), pp.1547-1565.

Bellaouar, A. and Elmasry, M., 2012. *Low-power digital VLSI design: circuits and systems*. Springer Science & Business Media.

Belorkar, M.U.A. and Ladhake, S.A., AREA EFFICIENT 3.3 GHZ PHASE LOCKED LOOP.

Bipin Gupta, Sanjay Rajak and Rahul Mishra 2014. Analysis of Leakage Power Reduction in PLL. *International Journal of Advanced Research in Computer Science & Electronics Engineering*,,3(5), pp. 258-262.

Brayton, R., Detjens, E., Phillips, N., Krishna, S., Ma, T., McGeer, P., Pei, L., Rudell, R., Segal, R., Wang, A. and Yung, R., 2003. Multiple-level logic optimization system. In *The Best of ICCAD* (pp. 191-203). Springer, Boston, MA.

Chung, C.C. and Lee, C.Y., 2003. An all-digital phase-locked loop for high-speed clock generation. *IEEE Journal of Solid-State Circuits*, *38*(2), pp.347-351.

Gothandaraman, A., 2004. Design and Implementation of an All Digital Phase Locked Loop using a Pulse Output Direct Digital Frequency Synthesizer.

Hathwalia, S. and Sankhyan, S.C., ULTRA-LOW POWER SUBTHRESHOLD CMOS INVERTER AT 90nm CMOS TECHNOLOGY.

Jasmin, M. 2014. Optimization Techniques for Low Power VLSI Circuits. *Middle-East Journal of Scientific Research*, 20(9), pp.1082-1087.

Kao, J.T. and Chandrakasan, A.P., 2000. Dual-threshold voltage techniques for low-power digital circuits. *IEEE Journal of Solid-state circuits*, *35*(7), pp.1009-1018.

Maffezzoni, P., Marucci, G., Levantino, S. and Samori, C., 2013. Comparing techniques for spur reduction in digital bang-bang PLLs. *Electronics Letters*, *49*(8), pp.527-529.

Minami, K., Fukaishi, M., Mizuno, M., Onishi, H., Noda, K., Imai, K., Horiuchi, T., Yamaguchi, H., Sato, T., Nakamura, K. and Yamashina, M., 2001, May. A 0.10/spl mu/m CMOS, 1.2 V, 2 GHz phase-locked loop with gain compensation VCO. In *Proceedings of the IEEE 2001 Custom Integrated Circuits Conference (Cat. No. 01CH37169)* (pp. 213-216). IEEE.

Parshionikar, S., Bhoir, D.V. and Prabhu, S., 2013. Leakage Power Reduction using Multi Threshold Voltage CMOS Technique. *International Journal of Scientific & Engineering Research*, *4*(10).

Ramakanth, K. and He, L., 2014. An Innovative Design of ADC and DAC Based Phase Locked Loop. In *Proceedings of the World Congress on Engineering* (Vol. 1).

Razavi, B., 2016. TSPC logic [a circuit for all seasons]. *IEEE Solid-State Circuits Magazine*, *8*(4), pp.10-13.

Rhee, W., 1999, May. Design of high-performance CMOS charge pumps in phase-locked loops. In *ISCAS'99. Proceedings of the 1999 IEEE International Symposium on Circuits and Systems VLSI (Cat. No. 99CH36349)* (Vol. 2, pp. 545-548). IEEE.

Silva-Pereira, M. and Vaz, J.C., 2018. Power optimization of both a high-speed counter and a retiming element for 2.4 GHz digital PLLs. *Electronics Letters*, *54*(5), pp.284-285.

Sirisantana, N., Wei, L. and Roy, K., 2000, September. High-performance low-power CMOS circuits using multiple channel length and multiple oxide thickness. In *Proceedings 2000 International Conference on Computer Design* (pp. 227-232). IEEE.

Tiebout, M., 2001. Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS. *IEEE Journal of Solid-State Circuits*, *36*(7), pp.1018-1024.
Wu, T., Hanumolu, P.K., Mayaram, K. and Moon, U.K., 2009. Method for a constant loop bandwidth in LC-VCO PLL frequency synthesizers. *IEEE Journal of Solid-State Circuits*, *44*(2), pp.427-435.

Wu, Y., Shahmohammadi, M., Chen, Y., Lu, P. and Staszewski, R.B., 2017. A 3.5–6.8-GHz Wide-Bandwidth DTC-Assisted Fractional-N All-Digital PLL With a MASH $\Delta\Sigma $-TDC for Low In-Band Phase Noise. *IEEE Journal of Solid-State Circuits*, *52*(7), pp.1885-1903.

Yun, S.J., Shin, S.B., Choi, H.C. and Lee, S.G., 2005, February. A 1mW current-reuse CMOS differential LC-VCO with low phase noise. In *ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005.* (pp. 540-616). IEEE.

MANAV RACHNA
Vidyanatariksha

Dr. O.P. Bhalla Central Library
Manav Rachna International Institute of Research and Studies
(A deemed-to-be-university under section 3 of UGC Act 1956)

SIMILARITY VERIFICATION CERTIFICATE

Title: **Novel Design of a Digital PLL for Power Reduction**

Researcher **Ms. Shruti Hathwalia**
Supervisor: **Prof. (Dr.) Naresh Grover**

Registration Number: **17/PhD/036**
Department : **ECE**

This is to certify that the above mentioned short synopsis was scanned for similarity index through **Turnitin** Software on **June 12, 2019** with submission ID **1142725269** and the similarity index was found to be **5 (Five)%**. The complete report running into 19 Pages, **3999 Word count** with File Size **4295 KB** is being forwarded to the Research Supervisor/DRC/DRB for review. The above report has been arrived after excluding attached five research papers co-authored with the Research Supervisor. Certificate of Exclusion of the same verified by the Research Supervisor has been attached.

Date: June 17, 2019

17/6/19
Dr. Vikram Kr. Sharma
University Librarian
Dr. O.P. Bhalla Central Library
Manav Rachna International
Institute of Research & Studies
Faridabad

The complete report of the above Short Synopsis has been reviewed and the similarity index is below the accepted norms as per the University Grants Commission (Promotion of Academic Integrity and Prevention of Plagiarism in Higher Educational Institutions) Regulations 2018. The short synopsis may be considered for further processing

17/6/19
Research Scholar

17/6
Research Supervisor

Shruti Hathwaliaa Short Synopsis June 12 2019

by Shrutii Hathwalia

Submission date: 12-Jun-2019 06:33AM (UTC+0530)
Submission ID: 1142725269
File name: Short_Synopsis_Shruti_Hathwalia_June_12_2019.docx (90.35K)
Word count: 3999
Character count: 21934

NOVEL DESIGN OF A DIGITAL PLL FOR POWER REDUCTION

SHORT SYNOPSIS

by

Shruti Hathwalia
17/Ph.D/036 (FET)

ABSTRACT

Very large scale integration (VLSI) circuits operating at ultra low power are currently acquiring more attention from the research group and the industries too. Recently, the performance of many applications depends on the size and energy consumption of sensor nodes. The sensor nodes with reduced size and energy efficient are much preferred among applications such as wireless sensor networks, pollution and plant monitoring, biomedical, smart grids. In present day digital systems, clocks are used for sequencing their operations and they also help in synchronization between different functional units.

The biggest challenge faced by the VLSI designers in present day life is designing a product of new generation which operates on minimum possible power. For preserving the power, it is required to achieve it with having high performance or minimal area. The new generation of designers should follow the design culture. The power consideration is the eventual design criteria in different real life applications like pacemakers etc. The main objective of all these applications is minimum power and maximum battery lifetime.

Shruti Hathwaliaa Short Synopsis June 12 2019

ORIGINALITY REPORT

Excluding matches less than 14 words

5%	3%	4%	3%
SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS

17/6/19

17/6/19.

PRIMARY SOURCES

1	Submitted to CSU, San Jose State University Student Paper	1%
2	Submitted to ABV-Indian Institute of Information Technology and Management Gwalior Student Paper	1%
3	University of Tennessee, Knoxville Publication	1%
4	www.it.pt Internet Source	1%
5	Submitted to Engineers Australia Student Paper	<1%
6	Submitted to Birla Institute of Technology Student Paper	<1%
7	Hyo-Hoon Park. "All-Digital Phase-Locked Loop for Optical Interconnect Applications", The 9th International Conference on Advanced Communication Technology, 02/2007 Publication	<1%

Vikram Kr. Sharma
Dr. O.P. Bhalla Central Library
Manav Rachna International
Institute of Research & Studies
Faridabad

8	etds.lib.ncku.edu.tw Internet Source	<1%
9	M. Silva-Pereira, J. Caldinhas Vaz. "Power optimisation of both a high-speed counter and a retiming element for 2.4 GHz digital PLLs", Electronics Letters, 2018 Publication	<1%
10	Submitted to Savitribai Phule Pune University Student Paper	<1%

Exclude quotes	On	Exclude matches	< 14 words
Exclude bibliography	On		